100G Coherent DWDM Interop and Pluggable Technology Review

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ABSTRACT

Bandwidth (BW) continues to grow in provider networks lead by video and multimedia services. Existing 10 and 40G DWDM interfaces are not meeting the scale requirements. 100G is becoming the prominent rate in Provider networks. Achieving 100Gig DWDM requires advanced modulation schemes as well as places a large emphasis on electronic compensation for linear network impairments to ensure both Brownfield as well as Greenfield deployments.

Providers are looking to decrease the cost of providing BW across the network. With the advent of 100Gig the cost curve has begun to shift from Switching to DWDM dominating cost per bit. It is felt that interop at the interface level of the DWDM optics will provide for greater competition as well as drive down the cost of 100G DWDM optics. Having interop will also help set the stage for achieving pluggable optics that will not only reduce cost but also increase face plate density. This document will address what is required to achieve interop as well as pluggable optics at 100Gig and is based on where we are today with respect to technology.

INTRODUCTION

Multiple attempts have been made to achieve a standard based implementation of 100G DWDM line side interfaces. The most successful attempt was in the OIF forum where the industry agreed on leveraging Dual Polarization-Quadrature Phase Shift Keying (DP-QPSK) modulation that leverages Coherent technology at the receiver that enables electronic compensation for linear network impairments, depicted in Figure 1 below.

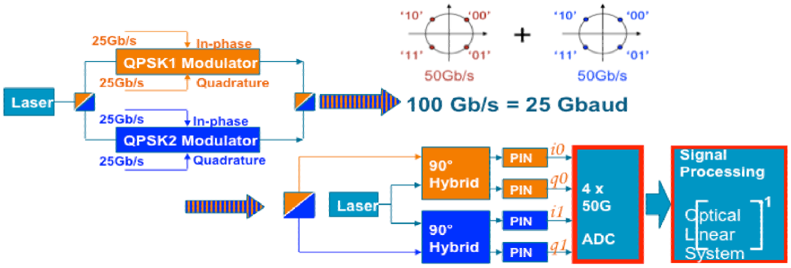

Figure 1: High Level depiction of DP-QPSK Transmit and Receive

Modulation standardization is a good start although does not provide the full mechanisms to allow for interop. Multiple Transmit, Line and Receive parameters need to be defined and standardized. ITU SG15 Q.6 has taken on this challenge at both 2.5G and 10G and successfully completed the effort and is defined in G.698.2, the reference network is depicted in Figure 2 below.

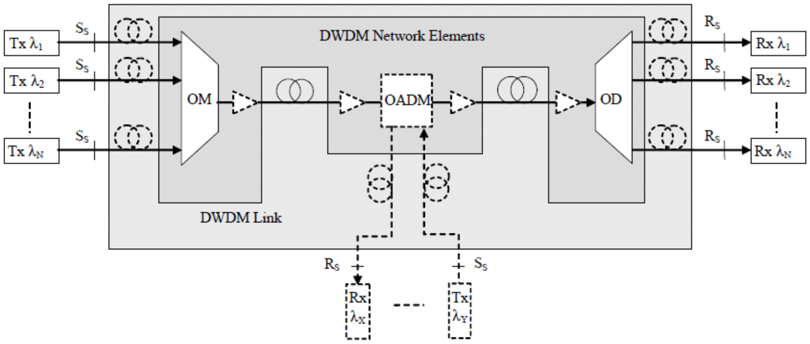

Figure 2: G.698.2 Reference network depicting points of standardization interest.

2.5G and 10Gig leveraged Non Return to Zero (NRZ) modulation, as such, the level of complexity in defining parameters to achieve standardization was a less challenging effort. At 100G, DP-QPSK introduces both Phase modulation and Polarization multiplexing which introduce a whole new dimension that had not to be addressed at 2.5 and 10G. At time of G.698.2, FEC had already been standardized further simplifying the effort, at 100G standard Reed Solomon (255,239) may not suffice for the distances needed. Even with existing G.698.2 standard, interop issues can still exist based on the multiple 10GE mapping options into OTN as well around EFEC, these such issues should be prevented at 100Gig.

The remainder of this document will take a closer look at what is required to be defined to ensure interop at 100Gig and close with an overview of what is needed to get to pluggable interfaces.

INTEROPERATION BETWEEN VENDORS

1.1 Different forms of Interop

Line side DWDM interop has been discussed for some time although has never fully come to fruition. DWDM systems used to be closed and run proprietary protocols to open and close ports, interfaces deployed different technologies to try and gain every fractional dB out of the interface since this was the differentiator, one interface was 'X'dB better then another venders. Providers pushed for greater openness and as such we ended up with open DWDM systems that support Alien or Foreign waves, an A-B-A type system depicted below in Figure 3.

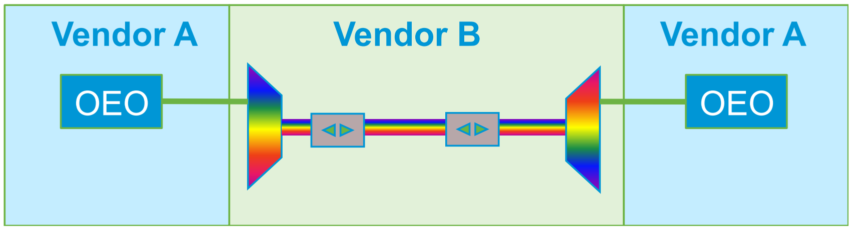

Figure 3: A-B-A – Alien wave system. Having the same DWDM interface vendor running over a third party DWDM system

The above model has been deployed and shown to be feasible in multiple Provider networks across the world. The next model of interest is the A-B-C model where we have a vendor A DWDM interface feeding in to a vendor B DWDM system terminating on a vendor C DWDM interface. Figure 4 below depicts this scenario which has been defined as Black Link in ITU G.698.2 for both 10G and 2.5G DWDM interfaces.

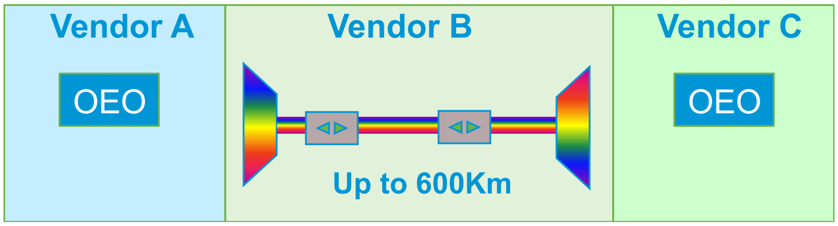

Figure 4: A-B-C – Black Link G.698.2 system with vendor A nd C DWDM interfaces running over yet another vendor DWDM system.

Challenges have been experienced with this model around 10G with respect to 10Gig E framing into OTU as well as going beyond the standard based RS(255,239) FEC coding. At 100G, with DP-QPSK and Coherent detection more challenges arise and more parameters must be defined to ensure interop. The remaining sections will focus on A-B-C interop since it will become evident that the requirements for A-B-A are a subset of A-B-C.

1.2 Parameters

The interface model depicted in Figure 5 highlights three key elements that must be accounted for during any standardization or interop effort.

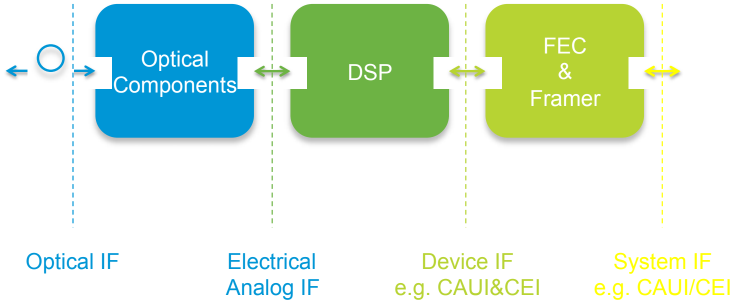

Figure 5: DP-QPSK with coherent detection interface model.

Utilizing the above interface model and focusing on three key aspects being General parameters, Transmit parameters and Receive parameters along with the already defined terms in ITU G.698.2 – Appendix A – it is felt that the following parameters are needing definition.

General Parameters:

DSP perspective, different vendors utilize different levels of coding of the digital signal in order to minimize effects of cycle slips caused from phase noise and similar effects as well as different acquisition techniques and leverage different techniques for carrier recovery and cycle slip detection. These parameters are above and beyond what is already defined in appendix A. Agreement will need to be reached around:

1. Coding – Leverage Differential encoding or non differential encoding to minimize probability of cycle slips
2. Carrier recovery / cycle slip detection – use or non use of pilot signals
3. Acquisition – blind acquisition or training sequence to lock on signal

From a FEC / Framer perspective, actual framing becomes an important parameter as well as the FEC algorithm which then leads into the distances needed to cover 600Km? 1000Km? etc… Agreement will need to be reached around:

1. Framing – OTU4.10, OTU4, etc….
2. Forward Error Correction – RS(255,239) will be very limited in reach capabilities at 100Gig. Need to agree on a strong enough FEC algorithm to meet typical distances. Staircase FEC case FEC is leading FEC option and is described in Appendix B.

Transmit Parameters:

Transmit characteristics will focus on mainly the Optical and DSP blocks of the interface model of Figure 5. Transmit characteristics become more challenging to measure due to the frequency of occurrence. The key parameters are dynamic in nature as such new terms need to be defined along with new algorithms.

One of the key terms to be defined is the Error Vector Magnitude (EVM). In simplest form, EVM is used to quantify the performance of a digital transmitter. Leveraging a reference constellation diagram, EVM specifies how far the actual constellation points may deviate from the reference hence ensuring a properly designed Receiver will receive the correct data points. Figure 6 below depicts the concept of EVM.

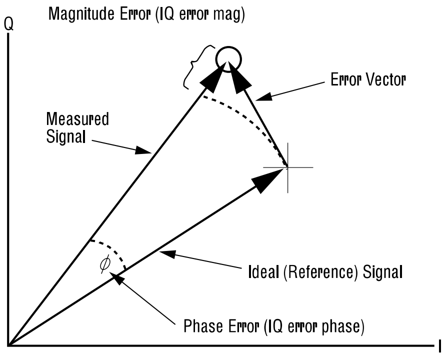

Figure 6: Error Vector Magnitude concept

Parameters to define include:

1. Optical Frequency Variation – peak variations in optical output frequency (optical phase variations – jitter in the time domain), tracking such variations will be very challenging as such developing tracking algorithm and having part of EVM measure becomes of interest.
2. Polarization Dependent Power – ensure that the orthogonal polarizations power variations are within reason.
3. Output Jitter – as of today there is no specification around output Jitter for 100G. This is relevant for the DSP section.
4. Constellation Diagram – part of EVM measure to set reference diagram. A two-dimensional scatter diagram representing a digitally modulated signal such as QPSK. Would be equivalent to the eye diagram in Amplitude modulated carriers.

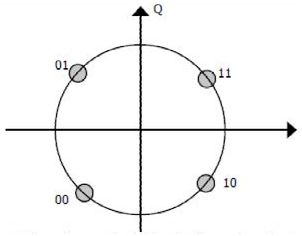

Figure 7: QPSK Constellation Diagram

Key parameters that would require focus would be the Optical Frequency variation as well as the Constellation diagram both of which can be addressed in the EVM measure although requires fast tracking algorithms to be developed / defined.

Receiver Parameters:

The receiver section focus is around the DSP in the interface model of Figure 5. Based on the Optical frequency variation of the transmit section above, one may correctly concluded as the EVM requires a fast tracking the Receiver will also require fast tracking mechanisms to track frequency variations. Tracking these variations becomes one of the key requirements of the standardization / interop effort. Tracking not only frequency variation but also polarization tracking will become instrumental as well.

Parameters to define include:

1. Optical frequency variation tolerance – speed of tracking frequency variations, or jitter tolerance in the time domain
2. Polarization variation tolerance – speed of tracking variation in polarization
3. Input Jitter tolerance – still needs to be defined for 100G

Key parameter to focus on would be the Optical frequency variation tolerance since this shall be the most challenging.

1.3 Summary of Interop / Standardization requirements

As of the date of this document, Cisco as well as others have attempted to achieve DWDM line side standardization in the OIF with some success in the form of a standardized modulation scheme being DP-QPSK. Working with DT, a joint contribution was made at the ITU SG15 Q.6 meeting in China on April 2012. The group had decided to take up the effort and use the preliminary parameters provided in the joint contribution. This effort will take time to achieve success due to some of the challenging parameters laid out above as well as the willingness of the industry to move forward quickly. It is felt achieving an A-B-A approach will pass sooner with minimum effort and set the stage for A-B-C. A-B-A provides Provider value in leveraging third party DWDM interface support and forcing more competitive situations and allows for advanced features to be developed. A-B-C will more likely be achieved by leveraging an ecosystem of partners and develop a common interface hence driving dual vendor interface interop. This will also provide clear Provider advantages.

When interop can be achieved we can then move into pluggable interfaces. Having pluggable interfaces by no mean provides vendor interop, standardization must come first although there are indeed advantages to pluggable technology include and not limited to footprint, power and path to reduced cost.

2. Conclusion

Achieving early interop at 100G will require leveraging partners to develop or share a common solution. Future interop will be based on standards such as the work taking place in the ITU SG15 Q6. Appendix A not only includes parameters but also proposed values of the parameters needing to be addressed by the standards body. Work must continue to drive the standards body to achieve a common transmission standard around 100Gig.

Appendix 1

	Units	Defined in clause x.y.z of G.698.2 in-force version	Proposed parameter
General information			
Minimum channel spacing	GHz	7.1.1	50
Bit rate/line coding of optical tributary signals	-	7.1.2	OTL4.4 DQPSK
Baud rate	Gbaud		27.952
Baud rate tolerance	Ppm		20
Data format			OTL4.4 on XI, XQ, YI and YQ
Framing			OTL4.x
FEC type*			Staircase Coded HG-FEC
FEC Coding Gain	dB		>=9.4
Error Floor			$<1e^{-20}$
Latency	us		<20
*Correction algorithm performance should not degrade in presence of correlated errors caused from advanced modulation schemes			
Data encoding			Differential Encoding '00' -> 180° '11' -> 0° '01' -> +-90° '10' -> -+90° See Note 1
Acquisition (blind training / sequence)			Blind
Maximum bit error ratio	-	7.1.3	10^{-12}
Fibre type	-	7.1.4	G.652, G.653, G.655
Interface at point S_S			
Maximum mean channel output power	dBm	7.2.1	+3
Minimum mean channel output power	dBm	7.2.1	-5

	Units	Defined in clause x.y.z of G.698.2 in-force version	Proposed parameter
Minimum central frequency	THz	7.2.1	191.7
Maximum central frequency	THz	7.2.2	196.1
Maximum spectral excursion	GHz	7.2.3	+- 1.8 GHz
Optical frequency variation ~~tolerance~~ $f_{mod} < 0.001$ Hz 0.001 Hz $<= f_{mod} < 0.1$ Hz 0.1 Hz $<= f_{mod} < 10$ Hz 10 Hz $<= f_{mod} < 1$kHz 1kHz $<= f_{mod} < 100$ kHz	MHz_{pp}		3000 9.48 MHz * $f^{-1/2}$ 300 948 MHz * $f^{-1/2}$ 30
Output jitter 20 kHz - 232 MHz 11.2 MHz - 232 MHz	UIpp UIpp		4.2 0.15
Tx polarization dependent power	dB		1.5
Error vector (including line width and equivalent eye diagram)			tbd
~~Constellation mapping~~	-	-	~~X~~
Minimum side mode suppression ratio	dB	7.2.4	30
Output OSNR	dB		40
~~Minimum channel extinction ratio~~	~~dB~~	~~7.2.5~~	~~NA~~
~~Eye mask~~	~~-~~	~~7.2.6~~	~~NA~~
Maximum transmitter (residual) dispersion OSNR penalty	dB	7.2.7	2
Optical path from point S_S to R_S			
Maximum ripple	dB	7.3.1	2
Maximum (residual) chromatic dispersion	ps/nm	7.3.2	20,000
Minimum (residual) chromatic dispersion	ps/nm	7.3.2	-5,000
Minimum optical return loss at S_S	dB	7.3.3	24
Maximum discrete reflectance between S_S and R_S	dB	7.3.4	-27
Maximum differential group delay	ps	7.3.5	100
Maximum polarization dependent loss	dB	7.3.6	2
Maximum inter-channel crosstalk at R_S	dB	7.3.7	tbd
Maximum interferometric crosstalk at R_S	dB	7.3.8	tbd
Maximum optical path OSNR penalty	dB	7.3.9	5
Minimum Guardband [1]	GHz		tbd

	Units	Defined in clause x.y.z of G.698.2 in-force version	Proposed parameter
Minimum Effective bandwidth	GHz		tbd
Interface at point R_S			
Data decoding	Tolerant against any swapping of OTL virtual lanes. Note 2		
Skewtolerance between virtual lanes	ns		1.6
Maximum mean input power	dBm	7.4.1	0
Minimum mean input power	dBm	7.4.1	-16
Minimum OSNR	dB (0.1nm)	7.4.2	22
Receiver OSNR tolerance	dB (0.1nm)	7.4.3	17
Maximum reflectance of receiver	dB	7.4.4	-27
Receive jitter 100 Hz < f_{mod} ≤ 20 kHz 20 kHz < f_{mod} ≤ 200 kHz 200 kHz < f_{mod} ≤ 5.6 MHz 5.6 MHz < f_{mod} ≤ 223 MHz	UIpp		 $8.4 \times 10^4 \times f^{-1}$ 4.2 $8.4 \times 10^5 \times f^{-1}$ 0.15
Rx optical frequency variation tolerance f_{mod} < 444 Hz 444 Hz <= f_{mod} < 100kHz 100kHz <= f_{mod} < 1 MHz	MHz_{pp}		 3000 $63.2 \times 10^3 \times f^{-1/2}$ 200
Polarization variation tolerance	rad/s		50,000

Note 1: It shall be allowed to encode ‘01’ int +90° and ‘10’ into -90° as well as to encode ‘10’ into +90° and ‘01’ into -90°. These two encodings result into a swapping of virtual lanes which shall be corrected by the receiver.

Note 2: It is desirable that the Receiver is tolerant also against a general inversion of the data into the differential encoder.

Note 3: It should not be assumed leveraging filter based multiplexers and demultiplexers as such Rx power monitoring shall be on a per channel basis not a composite power.

Appendix 2

This document adds details to clarify understanding of the proposed High-Gain FEC scheme and facilitate interoperable implementation. It also fixes minor typographical errors. The added Appendix ‘C’ includes the 12-stage P1 and P2 Permutation Maps referred to in the Error-Decorrelator function

1. INTRODUCTION

This is an update to the proposal for Hard Decision strong Forward-Error-Correction scheme (known as “Staircase” code) that addresses the Multi-vendor IaDI FEC for both OTU4 and “beyond 100G” transport signal rates (Metro FEC/”Black Link”). The same scheme can also be considered for use for “Beyond 100G” IrDI FEC in case better performance than G.709 OTUk RS(255,239) FEC is needed.

For the Metro FEC/"Black Link", the proposed "Staircase" Hard Decision FEC scheme has been demonstrated to give the reach and performance at a substantially lower cost than the Long Haul schemes for 100G and beyond transport signal rates typically using Soft Decision FEC.

What makes this attractive for the multi-vendor IaDI [Metro FEC/"Black Link"] for 100G and "Beyond 100G" are its demonstrated attributes:

- Higher Net Coding Gain
- Low error floor (flaring) makes this scheme very suitable for the Terabit future
- Verified performance in ASSP over Multi-lane interfaces and Complex Modulation schemes

For IrDI case for "Beyond 100G" – OTUCn, this proposal is attractive over the G.709 OTUk RS(255,239) FEC (also known as "GFEC") for reasons of performance and reuse (same FEC being used for MV-IaDI and IrDI).

The most common implementation for the proposed strong FEC "Staircase" code retains the default 6.7% overhead (also known as "7% overhead") as the RS(255,239) code in the G.709 standard for both multi-vendor IaDI and beyond 100G IrDI. Based on verified performance in ASSP, it outperforms all known G.975.1 codes in terms of

- coding gain (NCG>9.4dB)
- has low encoder/decoder implementation complexity
- low latency (<20us) and
- very low error floor (<1e-22)

This proposal adds a 20% Over-Head FEC "Staircase" scheme with similar structure to that of the 6.9% overhead (also known as "7% overhead") & G.709 compatible FEC that may be needed, for applications that require a higher Net Coding gain. Details of this scheme are covered in Section 2.6.

Appendices added in this contribution are provided to add further clarification and easier understanding of the overall scheme.

Appendix C provides a 12-stage P1 and P2 permutation map for the Interleaver. Permutation map for the De-Interleaver is not provided – but is easy to calculate – being that the De-interleaver is the inverse of the Interleaver.

2. DISCUSSION

2.1 Staircase Code Construction

Consider Fig. 1, in which each block B_i (for i a non-negative integer) is an m □ m array of symbols. *Staircase codes are characterized by the relationship between the symbols in successive blocks*

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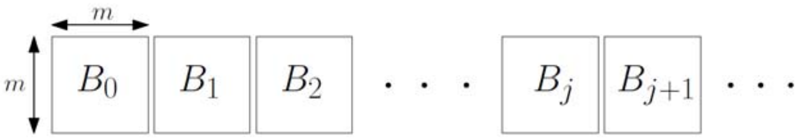

Figure 1: A stream of m □ m arrays of symbols.

First, we select a FEC code in systematic form to serve as the component code; this code, which we henceforth refer to as C, is selected to have block length $2m$ symbols, r of which are parity symbols. As illustrated in Fig. 2,the leftmost $2m-r$ symbols constitute information positions of C, the rightmost r symbols the parity positions of C. In light of this choice, we will find it useful to further sub-divide each block B_j into its $m - r$ leftmost columns and its r rightmost columns, as illustrated in Fig. 3, where $B_{j,L}$ is the sub-matrix consisting of the leftmost columns, and similarly for $B_{j,R}$.

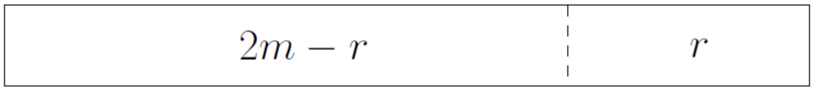

Figure 2: The sub-division of the length $2m$ systematic component codeword into its leftmost $2m - r$ information positions and its rightmost r parity positions.

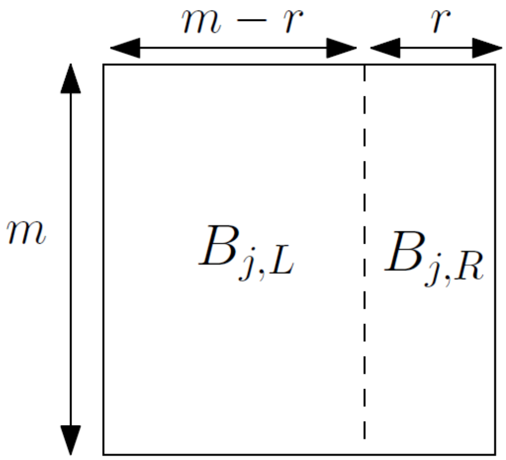

Figure 3: The sub-division of block B_j into its m-r leftmost columns and its r rightmost columns.

The $m(m-r)$ information symbols (from the streaming source) are arranged into $B_{j,L}$. Then, the entries of $B_{j,R}$ are specified as follows:

1. Form the m □ $(2m- r)$ matrix, $A =[B_{j-1}^T B_{j,L}]$, where B_{j-1}^T is the matrix-transpose of B_{j-1}.

2. The entries of $B_{j,R}$ are then computed such that each of the rows of the matrix $[B_{j-1}^T B_{j,L}\ B_{j,R}]$ is a valid codeword of C. That is, the elements in the lth row of $B_{j,R}$ are exactly the r parity symbols that result from encoding the $2m-r$ `information' symbols in the lth row of A.

Generally, the relationship between successive blocks in a staircase code satisfies the following relation: For any $i \geq 0$, *each of the rows of the matrix* $[B_i^T\ B_{i+1}]$ *is a valid codeword of* C.

An equivalent description-from which their name originates is suggested by Fig. 4, in which every row and every column in the `staircase' is a valid codeword of C. Note that these codes are naturally unterminated (i.e., their block length is indeterminate), and thus admit a range of decoding strategies with varying latencies.

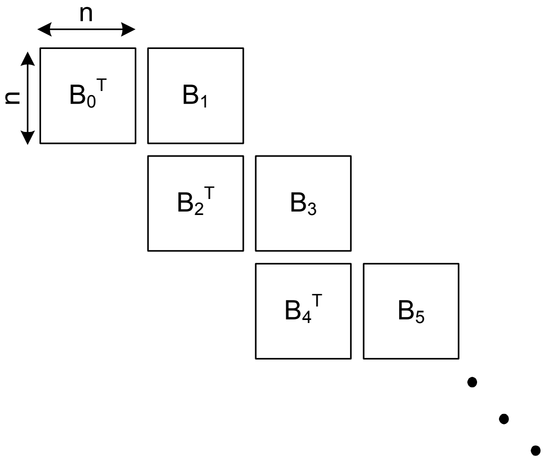

Figure 4: The `staircase' visualization of the family of staircase FEC codes.

2.2 Generalized Staircase Code Construction

To provide a straightforward mapping to the G.709 OTUk framing structure, it is useful to extend the definition of staircase codes to allow each block B_i (for i a non-negative integer) to be an $m \times n$ array of symbols, for $m \geq n$. As shown in Figure 5, $(m-n)$ rows of m zeros are appended to the top of the matrix B_i^T to create the matrix D_i^T, and f*or any* $i \geq 0$, *each of the rows of the matrix* $[D_i^T\ B_{i+1}]$ *is a valid codeword of* C. That is, the first (m-n) rows constitute shortened codewords.

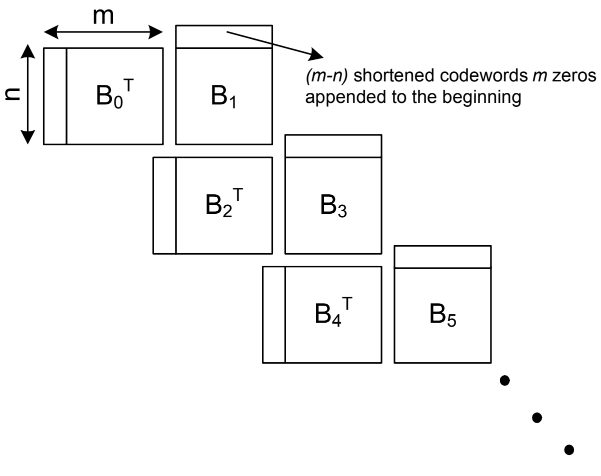

Figure 5: Generalized mxn staircase code

2.3 G.709-Compatible Generalized Staircase code

2.3.1 Encoding a 512x510 Generalized Staircase code

In a 512x510 generalized staircase code, each bit is involved in two triple-error-correcting (1022, 990) component codewords; the parity-check matrix H of the component code is specified in Appendix B.2. The assignment of bits to component codewords is described by first considering successive two-dimensional blocks $B_i, i \geq 0$, of binary data, each with 512 rows and 510 columns. The binary value stored in position $(\text{row, column}) = (j, k)$ of B_i is denoted $d_i\{j, k\}$.

In each such block, information bits are stored as $d_i\ \{j, k\}, 0 \leq j \leq 511, 0 \leq k \leq 477,$ and parity bits are stored as$\{j, k\}, 0 \leq j \leq 511, 478 \leq k \leq 509$. The parity bits are computed as follows:

1. For row $j, 0 \leq j \leq 1$, select $d_i\{j, 478\}, d_i\{j, 479\}, \dots, d_i\{j, 509\}$ such that

   $v = [0,0, \dots, 0, d_i\{j, 0\}, d_i\{j, 1\}, \dots, d_i\{j, 509\}]$
   satisfies

   $Hv^T = 0.$

2. For row $j, 2 \leq j \leq 511$, select $d_i\{j, 478\}, d_i\{j, 479\}, \dots, d_i\{j, 509\}$ such that

   $v = [d_{i-1}\{0, l\}, d_{i-1}\{1, l\}, \dots, d_{i-1}\{511, l\}, d_i\{j, 0\}, d_i\{j, 1\}, \dots, d_i\{j, 509\}]$
   satisfies

$Hv^T = 0,$
where $l = \Pi(j-2)$, and Π is a permutation function specified in Appendix B.1.

2.3.2 Mapping the 512x510 staircase code to G709 OTUk frame

The information bits in block B_i map to two G.709 OTUk frames, i.e., frames $2i$ and $2i+1$. The parity bits for frames $2i$ and $2i+1$ are the parity bits from block B_{i-1}. Each frame consists of 4 rows, and each row consists of 30592 information bits and 2048 parity bits. The information and parity bits to be mapped to each row, and their specific order of transmission, are specified as follows:

Information $d_i\{m \bmod 512, \lfloor m/512 \rfloor\}, 30592l \le m \le 30592l + 30591$

Parity $d_{i-1}\{m \bmod 512, 478 + \lfloor m/512 \rfloor\}, 2048l \le m \le 2048l + 2047$

The precise assignment of bits to frames, as a function of l, is as follows:

- Frame $2i$, row 1: $l = 0$
- Frame $2i$, row 2: $l = 1$
- Frame $2i$, row 3: $l = 2$
- Frame $2i$, row 4: $l = 3$
- Frame $2i+1$, row 1: $l = 4$
- Frame $2i+1$, row 2: $l = 5$
- Frame $2i+1$, row 3: $l = 6$
- Frame $2i+1$, row 4: $l = 7$

2.4 Decoding

Syndrome-based iterative decoding can be used to decode the received signal. Generation of the syndromes is done in a similar fashion to the encoding. The resulting syndrome equation is solved using the standard FEC decoding scheme and error locations are determined. Error locations are then flipped and standard iterative decoding proceeds. The latency of the decoder is a function of number of blocks used in the decoding process. Generally increasing the number of blocks improves the coding gain. The decoder can be configured in various latency modes to trade-off between latency and coding gain.

2.5 Performance

2.5.1 Coding gain and Latency

Extensive analysis using post-silicon OTU4 implementation of the Staircase code described above passing more than 1e18 bits through the decoder shows that the code performance closely matches the analysis.

Figure 5 shows the waterfall curve and Net Coding Gain for 2.25Mb latency OTUk decoder.

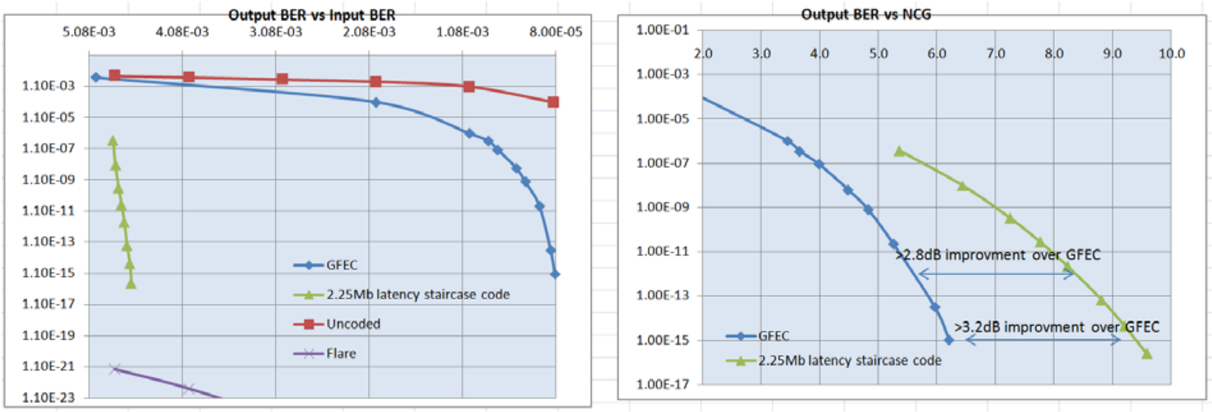

Figure 5: 2.25Mb latency OTUk Staircase Decoder

Lower latencies can be achieved at the expense of lower coding gain. Table 1 shows the trade-off between latency and coding gain

Latency	**BERi for BERo=1E-12**	**Net Coding Gain @1E-12**	**BERi for BERo=1E-15**	**Net Coding Gain @1E-15**
2.25Mb	4.70e-3	8.37dB	4.62e-3	9.41dB
2Mb	4.66e-3	8.36dB	4.55e-3	9.39dB
1.75Mb	4.62e-3	8.35dB	4.50e-3	9.38dB
1.5Mb	4.20e-3	8.25dB	3.80e-3	9.19dB

Table 1: Coding Gain/Latency trade-off

2.5.2 Flaring

In almost all iterative decoding schemes, there exist low probability error structures that cannot be corrected by the decoder. This induces “flaring” in the waterfall. For the proposed OTUk Staircase code the dominant stall pattern is a 16 bit 4x4 pattern. At the threshold input error rate of <5E-3, this will result in flaring of <1e-21. Post Silicon testing over very large payloads (>1e18) confirms the practical non-existence of the error flaring problem.

2.5.3 Burst error correction capability

The burst error correction capability of the proposed OTUk Staircase code is any combination of error bursts up to 1538 consecutive bits.

2.6 Error-Decorrelator function

Most forward-Error-Correction (FEC) codes are designed to perform under Additive White Gaussian Noise (AWGN), i.e., the decoder assumes that the noise samples are uncorrelated and Gaussian distributed. The performances of these codes can substantially decrease if the added noise is correlated. Error decorrelators can be added to FEC Encoder/Decoder to reduce the correlation of noise samples, thus approaching the performance under AWGN.

In conjunction with Staircase FEC Encoder/Decoder, the Error Decorrelator block can be used to randomize the position of the correlated error symbols to make sure the performance of the Staircase code is not impacted by correlated errors.

2.7.1 Error-Decorrelator function data path

Figure 7 shows the Error De-Correlator Datapath

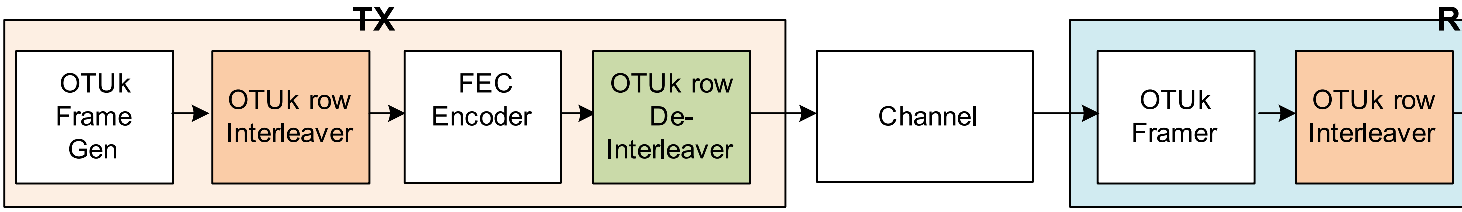

Figure 7:G.709 Compatible OTUk Error Decorrelator

Figure 8 shows the basic concept of the Interleaver/De-Interleaver. In this picture a 64-bit data stream is passing through a time varying permutation P1 filling a 64x64 block interleaver row-by-row. This block of data is then read column-by-column and passed through a 64-bit time-varying permutation P2. The controller controls the selection of the P1 and P2 maps.

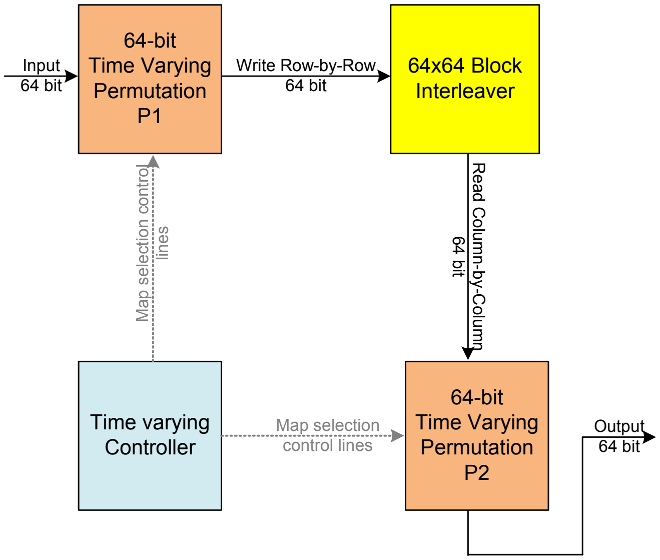

Figure 8: Simple example of Interleaver/De-Interleaver design

Figure 9 shows the block diagram for the implementation of P1 and P2

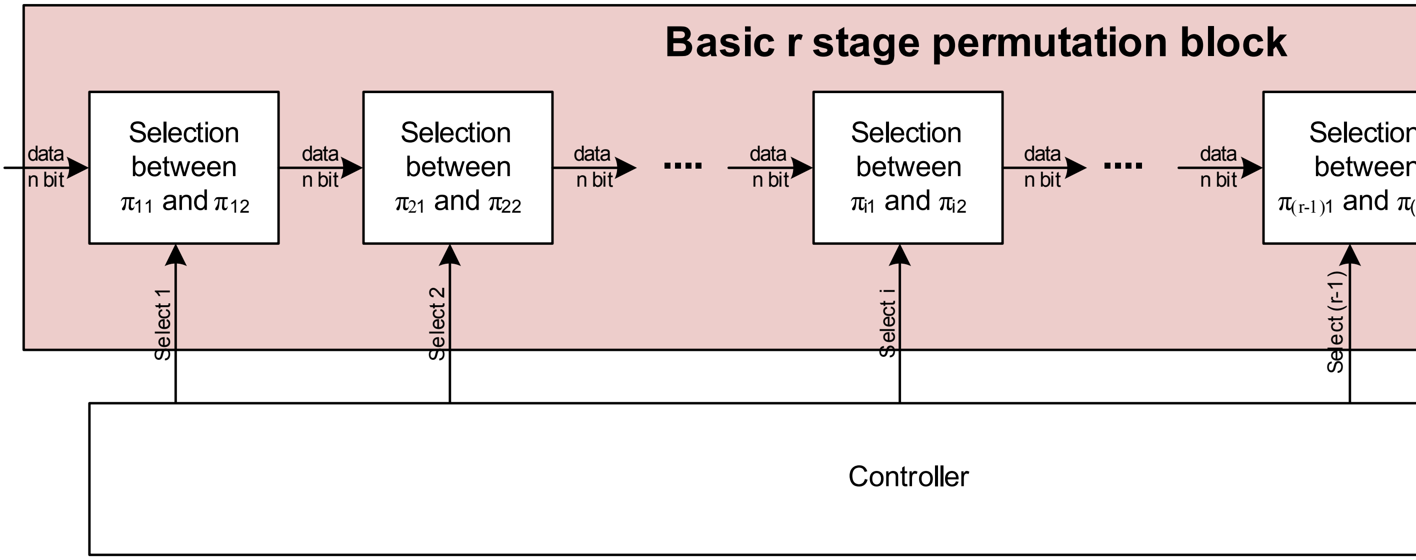

Figure 9: r stage permutation for P1 and P2

The permutation blocks P1 and P2 are designed through serial cascade of r elementary permutation functions. Each stage is selecting between one of the elementary permutations πi1, πi2.The select lines are dynamically changing resulting in a time varying permutation.

A fixed map or a choice of a few fixed maps can be used for the fixed block interleaver. Generally a matrix transpose is good choice for overall interleaver randomness.

2.7.2 G.709-Compatible Error Decorrelator

To make the Error Decorrelator compatible with G709 OTUk Row format, the interleaver/De-Interleavers are designed as follows

- Use 12 stage 64 bit permutation for P1 and P2 according to Appendix C.
- Use 40x64=2560 matrix transpose function for "fixed block interleaver" for the first 11 blocks of 2560 bits of data
- Use 38x64=2432 matrix transpose function for "fixed block interleaver" for the 12th block of data. (last data block)
- Use 32x64=2048 matrix transpose function for "fixed block interleaver" for the 13th block (parity block).

Note that 11x2560+2432=30592 which is the size of the data block in an OTUk row and 2048 is the number of parity bits in an OTUk row. With the proposed set of the fixed block interleavers, the data and parity are never mixed.

To control the P1 and P2, binary counters p1_cnt and p2_cnt can be used. p1_cnt can go from 1 to 4095 and p2_cnt can go from 1 to (4095-41). Since the number 41 is prime, the pair (p1_cnt, p2_cnt) will go through a large number of combinations before wrap around.

To synchronize the state of the controllers between the receiver and the transmitter, OTUk MFAS byte can be used. For example we can force (p1_cnt,p2_cnt)=(1,1) every time MFAS=0. Since MFAS is an 8-bit value, the total distinct number of control pairs is 256x4x32640/64=522,240 which is a large number resulting in a good overall randomization for the Error Decorrelator

3 PROPOSAL

We propose the OTUk staircase code together with the Error De-Correlator detailed in Section 2 of this contribution to become the baseline for both the 100G OTU4 Multi Vendor IaDI FEC (G.698.2) and "Beyond 100G" Multi Vendor IaDI FEC (Metro FEC/"black link", as an Annex to G.709.

In addition, if it is agreed that a stronger FEC than the current G.709 OTUk RS(255,239) FEC is needed for most "Beyond 100G" IrDI FEC transport applications, it is proposed that the same FEC scheme becomes the baseline for the "Beyond 100G" IrDI FEC.

In the event, no consensus is achieved around the 100G OTU4 Multi Vendor IaDI FEC, it may be worthwhile to consider a Supplemental appendix to G.709 (or possibly a G.sup) like collection that lists 100G OTU4 Multi Vendor IaDI FEC's. This would not be the most desirable outcome, but it would go some way to address the Multi Vendor IaDI FEC standardization and interoperability needs of Carriers.

Appendix A: Representation of elements in $GF(2^{10})$

For a root α of the primitive polynomial $p(\mathbf{x}) = \mathbf{1} + \mathbf{x}^3 + \mathbf{x}^{10}$, the non-zero field elements of $GF(2^{10})$ can be represented as

$\alpha^i \; 0 \le i \le 1022,$
which we refer to as the “power” representation. Equivalently, we can write

$\alpha^i = b_9\alpha^9 + b_8\alpha^8 + \cdots + b_{0,0} \le i \le 1022;$

we refer to the integer $l = b_9 2^9 + b_8 2^8 + \cdots + b_0$ as the “binary” representation of the field element. We further define the function $\log(\cdot)$ and its inverse $\exp(\cdot)$ such that for l, the binary representation of α^i, we have

$\log(l) = i$

and

$\exp(i) = l.$

Appendix B: OTUk compatible Staircase FEC code mapping

B.1 - Specification of Π

Π is a permutation function on the integers $i, 0 \leq i \leq 509$. In the following, $\Pi(M{:}M+N) = K{:}K+N$ is shorthand for $\Pi(M) = K, \Pi(M+1) = K+1, \ldots, \Pi(M+N) = K+N$. The definition of Π is as follows:

$\Pi(0{:}7) = 478{:}485$
$\Pi(8) = 0$
$\Pi(9{:}11) = 486{:}488$
$\Pi(12) = 1$
$\Pi(13) = 489$
$\Pi(14{:}16) = 2{:}4$
$\Pi(17{:}19) = 490{:}492$
$\Pi(20) = 5$
$\Pi(21) = 493$
$\Pi(22{:}24) = 6{:}8$
$\Pi(25) = 494$
$\Pi(26{:}32) = 9{:}15$
$\Pi(33{:}35) = 495{:}497$
$\Pi(36) = 16$
$\Pi(37) = 498$
$\Pi(38{:}40) = 17{:}19$
$\Pi(41) = 499$
$\Pi(42{:}48) = 20{:}26$
$\Pi(49) = 500$
$\Pi(50{:}64) = 27{:}41$
$\Pi(65{:}67) = 501{:}503$
$\Pi(68) = 42$
$\Pi(69) = 504$
$\Pi(70{:}72) = 43{:}45$
$\Pi(73) = 505$
$\Pi(74{:}80) = 46{:}52$
$\Pi(81) = 506$
$\Pi(82{:}128) = 53{:}99$
$\Pi(129) = 507$
$\Pi(130) = 100$
$\Pi(131) = 508$
$\Pi(132{:}256) = 101{:}225$
$\Pi(257) = 509$
$\Pi(258{:}509) = 226{:}477$

B.2 - Parity-check matrix

Consider the function f which maps an integer $i, 1 \leq i \leq 1023$, to the columnvector

$$f(i) = \begin{bmatrix} \beta_i \\ \beta_i^3 \\ \beta_i^5 \\ F(\beta_i) \\ \overline{F(\beta_i)} \end{bmatrix},$$

where

$$\beta_i = \alpha^{\log(i)},$$

and

$$F(\beta_i) = b_2^l \overline{b_1^l}\,\overline{b_0^l} \vee \overline{b_2^l} b_1^l \vee \overline{b_2^l}\,\overline{b_1^l} b_0^l,$$

for l the binary representation of β_i , and $\overline{x}$ is the complement of x. Then,

$$H = [\, f(1021) \;\; f(1022) \;\; f(1) \cdots f(510) \;\; f(511 + \Pi^{-1}(0)) \cdots f(511 + \Pi^{-1}(509))]$$

Appendix C: 12-stage P1 an P2 permutation maps

Each permutation stage is selecting between the two options of πi1 and πi2 as defined in section 2.6.1. We set all πi1's to identity mapping. The πi2 is selected from one of the five options by successively going through each option. At the start of the OTUk row option 1 is selected, the next clock option 2 is selected, the next clock option 3 is selected, the next clock option 4 is selected, the next clock option 5 is selected and then roll over back to option 1 and repeat all the way to the end of the OTUk row.

Mapping for P1, Option1 for the 12 stages are shown in 64x12 matrix P1_1
Mapping for P1, Option2 for the 12 stages are shown in 64x12 matrix P1_2
Mapping for P1, Option3 for the 12 stages are shown in 64x12 matrix P1_3
Mapping for P1, Option4 for the 12 stages are shown in 64x12 matrix P1_4
Mapping for P1, Option5 for the 12 stages are shown in 64x12 matrix P1_5

Mapping for P2, Option1 for the 12 stages are shown in 64x12 matrix P2_1
Mapping for P2, Option2 for the 12 stages are shown in 64x12 matrix P2_2
Mapping for P2, Option3 for the 12 stages are shown in 64x12 matrix P2_3
Mapping for P2, Option4 for the 12 stages are shown in 64x12 matrix P2_4
Mapping for P2, Option5 for the 12 stages are shown in 64x12 matrix P2_5

The De-Interleaver is the inverse of the Interleaver. We only define the Interleaver map here.

P1_1=

26	16	45	6	6	43	35	30	38	32	14	4
9	3	31	49	9	9	59	8	22	13	30	11
27	60	42	1	12	39	57	28	15	52	16	35
49	63	52	62	15	22	27	49	63	9	55	18
16	31	5	16	63	10	29	63	62	42	34	43
14	23	3	36	30	35	30	52	58	1	32	42
10	46	26	52	29	42	3	13	4	3	15	63
56	32	4	61	51	1	62	14	30	55	61	59
45	28	0	2	23	12	36	56	5	63	22	53
51	62	12	30	45	21	18	25	21	12	9	39
11	42	17	31	46	56	56	59	48	59	44	51
55	7	59	32	8	53	41	47	18	40	39	37
40	41	27	20	50	57	13	58	52	26	36	57
46	9	10	28	37	45	42	33	37	30	24	2
62	10	2	47	2	36	45	36	20	17	50	47
35	13	9	8	22	32	16	17	0	57	5	15
7	33	44	54	32	48	2	20	59	19	58	0
1	59	51	55	13	50	11	11	61	49	63	36
21	24	30	46	41	38	53	16	28	25	4	32
50	2	8	33	47	54	47	48	27	53	10	5
12	1	54	29	10	63	17	41	16	10	23	3
42	35	22	43	3	27	49	51	19	6	49	14
63	18	18	7	36	26	60	62	12	62	46	60
25	21	38	50	4	59	7	60	2	27	47	9
48	49	33	39	17	30	50	38	49	50	42	13
43	22	23	15	54	11	44	1	31	28	29	38
0	14	49	60	28	46	0	19	41	2	8	30
5	15	1	10	53	31	26	29	32	8	52	25
47	27	41	22	49	37	21	9	14	45	11	44
4	5	32	59	61	13	28	57	36	33	38	28
58	4	20	18	38	28	22	46	26	60	26	61
6	25	53	37	39	55	37	40	51	56	2	58
29	38	63	51	5	49	33	6	45	41	7	20
13	17	21	24	44	41	15	31	54	0	31	45
60	29	48	27	56	8	54	34	1	58	17	56
61	12	6	34	25	34	24	22	53	29	35	6
38	6	50	38	52	40	1	55	44	46	19	54
31	43	36	53	59	51	6	12	29	31	3	19
8	39	58	26	7	3	55	35	33	16	37	46
23	57	39	9	27	17	34	7	56	36	53	33
57	58	34	14	35	4	63	39	10	23	40	62
33	26	13	4	1	29	58	50	7	15	1	52
22	19	35	44	20	58	39	54	8	11	18	31
19	11	47	42	21	44	32	21	47	18	45	40
38	49	14	59	4	33	10	50	9	34	18	49
53	44	24	11	26	16	46	27	40	51	54	23
34	8	55	48	60	18	43	4	23	39	59	50
32	61	7	17	18	19	61	0	42	38	20	55
15	54	43	58	48	60	23	32	6	61	6	34
17	0	14	5	42	5	4	3	55	43	43	27
2	47	16	63	62	6	12	5	46	48	41	10
30	56	37	41	0	24	5	10	25	35	21	22
28	20	56	35	58	61	51	61	57	24	27	29
44	36	46	40	16	14	14	2	24	54	60	24
24	34	60	45	34	47	48	26	60	20	62	41
37	40	15	56	11	23	9	45	9	4	25	49
54	48	62	13	40	52	19	43	34	22	0	1

39	50	40	12	19	33	25	23	11	5	12	8
52	55	29	57	24	7	52	37	39	44	48	26
18	30	28	3	31	20	38	53	35	7	57	21
3	37	19	19	43	62	20	42	13	21	28	7
59	45	25	0	33	25	10	18	3	34	56	48
36	53	11	21	55	15	8	44	17	47	51	17
20	52	57	23	57	0	40	24	50	14	33	12

P1_2=

37	8	25	40	34	50	31	53	4	18	34	55
45	33	3	31	29	12	24	42	23	25	8	31
44	52	46	54	63	57	55	61	52	12	20	50
20	5	52	5	8	45	16	43	19	33	56	26
23	14	24	22	36	4	40	7	59	15	7	40
42	41	31	39	35	26	49	11	27	6	40	17
52	50	45	56	16	47	54	46	35	35	54	16
53	26	61	44	22	44	18	55	56	61	51	42
19	20	2	9	11	31	12	57	44	22	15	63
39	40	44	16	6	49	61	20	28	43	44	45
36	32	48	25	25	14	29	32	18	0	38	51
41	30	18	28	19	59	50	40	8	41	22	3
48	3	19	18	38	7	37	37	3	19	31	32
31	62	30	46	61	62	59	62	39	16	12	61
43	36	26	45	58	36	63	51	31	14	28	4
25	21	20	49	17	53	19	60	6	40	36	12
30	47	4	55	56	10	23	0	10	37	39	53
4	22	49	58	28	38	39	10	15	39	46	27
59	10	9	32	57	23	46	8	46	32	6	11
0	39	23	21	54	35	27	29	51	38	45	62
21	28	57	30	62	18	33	41	40	26	63	1
15	9	8	36	24	25	11	17	20	42	17	13
28	6	1	35	59	60	36	15	0	13	55	57
16	46	38	20	55	34	41	9	2	27	4	24
27	42	58	4	44	40	58	27	63	29	50	8
61	56	0	6	1	37	57	63	1	48	3	54
63	55	55	8	14	39	4	22	24	60	53	37
58	37	28	23	9	29	3	14	25	31	48	35
17	27	21	38	45	8	9	16	22	51	26	43
26	53	17	48	27	15	20	45	30	10	2	7
60	12	35	52	20	41	56	52	7	53	29	14
3	4	42	37	46	11	6	18	45	17	62	33
7	63	39	53	47	48	8	59	49	20	58	9
13	54	22	57	21	55	47	30	62	5	47	58
12	16	43	43	2	22	38	47	32	55	5	2
46	60	5	3	53	43	17	35	21	58	60	15
57	29	59	2	51	9	53	44	5	54	16	56
9	17	10	33	23	20	2	12	12	7	42	30
24	0	37	42	52	17	15	36	36	49	23	48
2	45	33	19	12	28	5	33	57	36	13	34
14	48	36	29	43	63	25	39	61	59	9	59
55	58	12	7	39	6	44	28	37	62	24	19
22	38	32	24	18	16	26	49	55	23	49	6
10	19	40	41	60	46	21	1	16	46	61	44
29	39	0	1	59	43	49	38	16	34	7	32
40	44	63	51	3	2	62	5	17	1	11	38
54	61	13	63	32	24	43	25	53	56	0	22
8	15	53	14	40	27	45	4	11	3	27	25
50	25	56	60	48	58	13	48	41	11	33	36
33	13	16	50	49	13	1	34	43	2	10	39
35	24	27	11	7	32	51	13	47	30	37	46

29	57	54	15	33	52	34	26	33	57	14	21
5	7	15	26	30	1	48	38	42	8	32	10
56	59	47	10	42	5	30	24	48	52	35	47
34	35	50	62	13	61	22	21	38	9	52	52
6	1	11	0	41	30	32	19	54	24	57	60
32	23	51	27	0	19	35	3	60	4	21	41
11	11	60	17	37	21	52	6	26	47	41	20
47	51	6	34	50	0	7	54	34	45	59	29
62	31	41	47	10	56	42	56	50	28	25	5
18	34	62	13	31	3	0	31	14	63	19	28
51	18	29	1	15	42	14	2	58	21	30	18
1	43	34	61	26	54	60	23	13	50	43	0
49	2	7	12	5	51	28	58	29	44	1	23

P1_3=

46	1	28	58	55	38	7	9	33	2	34	42
21	41	46	24	60	58	13	8	60	35	42	61
37	20	19	53	33	54	17	28	44	61	38	0
6	21	16	5	39	19	18	1	55	9	54	19
41	62	54	63	11	20	40	49	21	52	31	45
52	56	59	9	53	11	48	31	0	43	56	37
10	15	34	47	36	7	25	12	24	13	32	30
9	28	1	18	42	5	24	14	46	17	51	39
32	11	36	17	28	57	60	3	37	10	8	56
58	57	13	19	63	53	2	45	51	27	46	6
28	31	56	62	27	59	5	36	35	46	16	49
7	36	32	55	46	21	8	16	22	25	25	16
24	48	12	32	13	8	41	21	12	32	1	15
22	63	48	45	0	55	43	48	41	14	12	46
34	10	10	2	47	62	0	32	28	57	26	44
33	52	58	57	7	12	53	33	11	49	23	27
54	6	39	27	26	41	30	63	58	1	53	21
31	4	21	29	45	22	36	15	30	54	4	40
60	19	53	39	9	56	29	52	42	16	58	24
47	24	22	48	51	37	6	59	27	44	30	18
3	47	30	54	41	40	56	35	63	24	48	48
38	42	8	34	31	29	39	34	31	30	41	25
12	55	42	33	49	49	20	57	47	60	13	23
19	60	5	6	23	27	15	13	26	38	35	31
48	34	47	4	17	63	54	5	57	31	43	54
5	35	37	60	12	10	51	19	50	23	45	62
25	14	40	61	2	4	58	37	61	59	20	17
57	13	44	12	10	26	16	42	7	37	11	38
35	33	63	15	22	60	50	55	32	8	5	26
39	26	62	10	35	44	22	26	10	51	17	9
23	32	50	8	56	34	55	56	19	50	6	10
44	25	61	28	52	1	23	23	2	48	3	12
36	40	3	13	20	25	38	18	4	4	37	41
56	3	29	40	1	9	34	41	25	40	29	50
17	50	35	14	48	51	19	27	43	20	27	47
43	45	2	36	16	13	59	44	40	12	19	58
11	51	9	31	21	52	4	60	39	22	40	28
27	30	4	25	30	35	12	6	62	3	14	29
16	0	14	7	43	39	10	30	3	42	22	33
30	8	11	35	50	42	27	10	14	58	44	11
59	9	51	44	57	61	45	24	59	26	61	59
18	46	33	59	32	3	33	0	23	55	18	36
13	44	23	50	37	32	62	43	17	56	21	34
4	27	52	46	5	36	46	29	6	62	28	63
58	57	47	43	11	45	37	49	27	54	0	32

53	58	38	49	58	2	14	39	1	53	62	1
1	5	7	0	40	18	9	47	9	63	15	20
50	12	26	20	61	50	11	62	54	41	52	35
51	22	45	43	3	45	63	2	15	18	59	53
20	61	24	51	62	0	61	54	34	33	50	52
62	38	27	30	19	30	44	46	8	6	33	7
63	17	49	42	29	17	37	61	56	47	36	43
55	43	18	3	44	33	3	20	45	11	9	2
2	16	60	52	4	47	31	7	13	29	57	8
45	29	25	22	24	6	57	40	53	28	63	13
8	59	43	56	15	28	42	25	48	7	10	60
42	54	55	38	14	31	47	53	36	45	60	5
49	53	20	16	18	23	32	22	49	39	49	55
26	37	17	11	54	46	28	58	20	36	39	4
61	23	41	21	34	24	21	50	52	5	24	22
15	49	31	37	8	15	1	11	18	15	47	57
0	7	6	26	6	16	52	4	5	19	0	14
40	2	57	23	38	48	26	17	38	21	2	3
14	18	15	41	25	14	35	51	29	0	55	51

P1_4=

47	10	18	49	22	3	45	39	48	56	7	25
30	29	43	14	43	16	57	7	57	62	12	2
3	32	58	1	35	1	7	54	11	5	2	52
60	35	8	39	62	46	8	0	16	57	15	42
18	27	4	5	36	55	40	24	14	60	9	55
50	39	44	48	61	13	32	19	50	3	19	39
62	48	55	16	33	50	20	2	33	45	22	51
45	56	48	38	49	26	59	21	38	49	47	57
54	16	15	10	38	15	1	44	49	7	18	35
0	50	61	46	12	60	41	46	21	63	23	62
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